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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/763,868	02/28/2001	Michel Hazard	T2146-906833	3510

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EXAMINER	
TRAN, TONGOC	

ART UNIT	PAPER NUMBER
2134	

DATE MAILED: 09/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/763,868	HAZARD, MICHEL	
	Examiner	Art Unit	
	Tongoc Tran	2134	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20,21,23-31 and 33-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20,21,23-31 and 33-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to Applicant's amendment filed on 6/9/2006. Claims 20, 21, 23-31 and 33-36 have been amended. Claims 22 and 32 have been canceled. Claim 39 has been added. Claims 20, 21, 23-31 and 33-39 are pending.

Response to Arguments

2. In response to Applicant's arguments filed 6/9/2006 stated that the cited prior art Holtey fails to teach or suggest "any logic verification operations being applied to all bits of said datum transmitted on said data bus...the detection of the alteration of any bit of datum transmitted on a bus" (remark, page 8). Holtey teaches a microprocessor (processing device) interconnected through an internal bus (data bus) to a memory chip (storage device) for transmitting address, data and control information (datum) (col. 2, lines 55-67); Holtey further teaches security logic circuit (logic verification operations) for performing comparison of each bits of a key value against the bit contents of lock bit positon of the memory block read out in response to instruction. The amended claimed language recites the selected information is to be transmitted on the data bus or the processing of the datum on the all bits of said datum which is transmitted on said data bus. Since the information taught by Holtey is transmitted between the memory chips and the processor, it is reasonably interpreted that the integrity check is performed on the data which is channel through the data bus. In light of this interpretation, Examiner maintained the rejections for claims 20 and 29.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 24 and 25 recite the limitation "wherein said logic" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 20 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Holtey (U.S. Patent No. 5,442,704).

In respect to claim 20, Holtey discloses a method for protecting the processing of sensitive information in a security module having a monolithic structure, comprising at least an information processing device, for storing information capable of being processed by said processing device, mans for checking the integrity of information and at least a data bus wherein the transmitting of information through said data bus is secured by at least the following steps (see Abstract):

selecting a piece of sensitive information stored in the storage device; determining a specific condition for the integrity of a datum transmitted from the storage

device to processing device on said data bus; processing said datum and executing a logic verification operation on all bits of said datum which is transmitted on said data by the processing device or by the means on said data bus by the processing device or the means for checking the integrity of information, during processing device or by the means for checking the integrity of information, during the processing for verifying that the specific condition is satisfied; and disabling the processing device if the specific condition is not satisfied (see Fig. 1, col. 3, line 15-col. 4, line 49 and col. 5, line 39-col. 6, line 35).

In respect to claim 29, the claim limitation is a system claim that is substantially similar to method claim 1. Therefore, claim 29 are rejected based on the similar rationale.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20, 21, 26-31, 33, 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Geronimi et al. (U.S. Patent No. 5,465,349, hereinafter Geronimi) in view of Kommerling et al. ("Design Principles for Tamper-Resistant

Smartcard Processors", USENIX Worship on Smartcard Technology, May 10-11, 1999, hereinafter Kommerling).

In respect to claims 20, 21, 26, 27, 30, 31, 37 and 38, Geronimi discloses a method for protecting the processing of sensitive information in a security module having a monolithic structure, comprising at least an information processing device, for storing information capable of being processed by said processing device, mans for checking the integrity of information and at least a data bus wherein the transmitting of information through said data bus is secured by at least the following steps:

Geronimi discloses performing testing to check the environment conditions and the conditions of operation of the circuit in order to prevent fraudulent operations (see col. 2, lines 18-52 and col. 3, lines 18-40); During the processing for verifying that the specific condition is satisfied; and disabling the processing device if the specific condition is not satisfied (see col. 2, lines 18-52 and col. 3, lines 18-40).

Geronimi does not disclose the detail of how the testing is check. However, Kommerling discloses environment attack on smartcard may alter critical machine instruction with arbitrary one (see Kommerling, 2.2.1). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the teaching of Geronimi's testing of environmental conditions and the condition of operation of the circuit to prevent fraudulent operations to encompass comparing verifying the critical instruction accessing by the processor to ensure that these critical instruction has not be altered during the accessing from the memory to the processor.

In respect to claim 29, the claimed invention is similar to claim 20. Therefore, claim 29 is rejected based on the similar rationale.

In respect to claims 28 and 33, Geronimi and Kommerling further disclose reading by the processing device said nonvolatile location of the storage device upon power up of said module before disabling the processing device if a value read at this location does not match (see Geronimi, col. 1, lines 50-63).

6. Claims 23-25, 34-36 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Geronimi et al. (U.S. Patent No. 5,465,349, hereinafter Geronimi) in view of Kommerling et al. ("Design Principles for Tamper-Resistant Smartcard Processors", USENIX Worship on Smartcard Technology, May 10-11, 1999, hereinafter Kommerling) and further in view of Coyle et al. (U.S. Patent No. 6,502,212, hereinafter Coyle).

In respect to claims 23, 34 and 39, Geronimi and Kommerling do not explicitly disclose but Coyle wherein said means for checking the integrity of said information comprises a logic comparator and a first and second logic operator disposed each at different termination of the data bus, said logic operators producing at least respectively a first and a second result compared together by said logic comparator for verifying said specific condition for the integrity when there is an equality between said first said second results (see Coyle, Fig. 1, col. 6, line 45-col. 7, line 27). It would have been

obvious to one of ordinary skill in the art at the time the invention was made to implement the logic comparator taught by Coyle for testing bus error.

In respect to claims 24-25 and 35-36, Geronimi, Kommerling and Coyle further disclose a logic selection input of both comparators is set to calculation data whose value varies as a function of time/randomly (see Kommerling, page 8, 3.1).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tongoc Tran whose telephone number is (571) 272-3843. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-3962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TT
September 5, 2006

GILBERTO BARRON JR.
SUPERVISORY PATENT EXAMINER
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